REMARKS

Claims 1-4, 6-8, 11-13, 15-21 and 23 are pending. The Applicant respectfully requests reconsideration of the Claims based on the discussion presented below.

35 U.S.C. §102

Claims 1-4, 7-8, 12-13, 16-21 and 23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Kadanka et al. (U.S. Patent No. 5,621,308). Applicants have reviewed the recited references and respectfully submit that the present invention, as is recited in Claims 1-4, 7-8, 12-13, 16-21 and 23, is neither anticipated nor rendered obvious by Kadanka et al. either alone or in combination.

The Examiner is respectfully directed to independent Claim 1 which is drawn to a band-gap reference circuit. Claim 1 is reproduced below in its entirety for convenience of the Examiner.

> 1. A band-gap reference circuit, comprising:
> a band-gap reference unit;
> a buffer circuit electronically coupled with said band-gap reference unit; and
> a single component voltage pull-up device that is separate from said band-gap reference unit electronically coupled between said band-gap reference unit and said buffer circuit, wherein said voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference voltage and wherein said voltage pull-up device is implemented as a transistor.

Claims 7 and 16 recite limitations similar to those recited in Claim 1. Claims 2-4 depend from claim 1 and recite additional limitations of the claimed invention. Claims 8, 12-13 depend from claim 7 and recite additional limitations of the claimed invention. Claims 17-21 depend from claim 16 and recite additional limitations of the claimed invention.

Kadanka et al. does not anticipate or render obvious the embodiment of the claimed invention that is set forth in Claim 1 (Claims 7 and 16 recite limitations similar to those recited in Claim 1). Kadanka et al. is deficient as Kadanka et al. does not teach or suggest a band-gap reference circuit that includes "a single component voltage pull-up device that is separate from said band-gap reference unit electronically coupled between said band-gap reference unit and said buffer circuit ...wherein said single component voltage pull-up device is implemented as a transistor" as is recited in Claim 1 (Claims 7 and 16 recite limitations similar to those recited in Claims 7 and 16).

In order to meet the limitations of Claim 1 (Claims 7 and 16 contain similar limitations) a reference must teach or suggest either expressly or inherently, along with other limitations of the Claim 1: (1) a single component voltage pull-up device that is separate from a band-gap reference unit, (2) a band-gap reference unit, and (3) a buffer circuit.

Applicant understands Kadanka et al. as disclosing a dissimilar electrical apparatus for providing a reference signal that includes a regulator portion that provides a substantially constant current. It is important to note that Kadanka et al. simply does not discuss a buffer circuit or a voltage pull-up device. In fact, Kadanka et al. discloses that element 57, cited in the Office Action as being equivalent to the recited voltage pull up device, is actually a part of bandgap reference circuit 72. This is contrasted with the express provisions of Applicant's Claims that require that the pull-up device not be a part of a bandgap reference circuit.

In the instant rejection, the Examiner equates portions of bandgap reference unit 72 disclosed by Kadanka et al. to the recited bandgap reference unit of Applicant's Claim 1. Other portions of bandgap reference unit 72 are equated to the recited voltage pull-up device of Applicant's Claim 1. This interpretation of Kadanka et al. is the basis for the Examiner's

contention that Kadanka et al. teaches a voltage pull-up device that is separate from a band-gap reference unit such as is required to meet the limitations of Claim 1 (Claims 7 and 16 recite similar limitations). Applicant's strongly disagree with the Examiner's interpretation of the Kadanka et al. reference. Applicant respectfully submits that the Examiner's interpretation is at odds with what is clearly disclosed by Kadanka et al. More specifically, Kadanka et al. discloses in the clearest manner possible the elements that are considered to be a part of bandgap reference unit 72, and transistor 57 (which as discussed above is equated by the Examiner to the recited voltage pull-up device) is shown as actually being a part of bandgap reference unit 72. Referring now to Figure 2 of Kadanka et al., the components that are considered to be a part of bandgap reference unit 72 are clearly delineated through circumscription using a dashed line. Transistor 57 is unmistakably shown as lying within the dashed line.

As transistor 57 is a part of the bandgap reference unit 72 of Kadanka et al., it cannot reasonably be equated to the recited voltage pull-up device of Applicant's Claim 1 that is delimited as being separate from the recited bandgap reference unit of Applicant's Claim 1. Accordingly, the prima facie case for anticipation upon which the instant rejection is based is clearly deficient.

Moreover, Applicant respectfully submits that nowhere in the Kadanka et al. reference is a single component voltage pull-up device that is separate from a band-gap unit and that is electronically coupled between a band-gap reference unit and a buffer circuit as is set forth in Claim 1 and disclosed in the Applicant's specification, taught or suggested. Consequently, the embodiments of the claimed invention as are set forth in independent Claims 1, 7 and 16 are neither anticipated nor rendered obvious by Kadanka et al.

Moreover, as it regards limitations recited in Claim 2, Applicant respectfully submits that nowhere in the Kadanka et al. reference is a method of responding to a request for a key of a first length that includes the above discussed limitation of Claim 1 and further includes the limitations "wherein said band-gap reference circuit resides in an integrated circuit device" as is recited in Claim 2 taught or suggested. Additionally, as it regards limitations recited in Claim 3, Applicant respectfully submits that nowhere in the Kadanka et al. reference is a method of responding to a request for a key of a first length that includes the above discussed limitation of Claim 1 and further includes the limitations "wherein said band-gap reference circuit is implemented in a silicon substrate" as is recited in Claim 3 taught or suggested. And, as it regards limitations recited in Claim 4, Applicant respectfully submits that nowhere in the Kadanka et al. reference is a method of responding to a request for a key of a first length that includes the above discussed limitation of Claim 1 and further includes the limitations "wherein said buffer circuit is implemented as a transistor" as is recited in Claim 4 taught or suggested.

Because of the deficiencies of Kadanka et al. discussed above, Applicant respectfully submits that Kadanka et al. does not provide an adequate basis for rejection of Claims 1, 7 and 16 under 35 U.S.C. §102 and, as such, Claims 1, 7 and 16 are allowable. Accordingly, the Applicant respectfully submits that Claims 2-4, 8 and 12-13 and 17-21, dependent on Claims 1, 7 and 16 respectively, are likewise allowable as being dependent on allowable base claims.

35 U.S.C. §103

Claims 6, 11, 15 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kadanka et al. (U.S. Patent No. 5,621,308) in view of Mietus (U.S. Patent No. 5,666,046). Applicant has reviewed the cited references and respectfully submit that the embodiments of the claimed invention, as are set forth in Claims 6, 11, 15 and 23, are neither anticipated nor rendered obvious by Kadanka and Mietus, either alone or in combination. Mietus does not teach

or suggest a modification of Kadanka et al. that would remedy the deficiencies of Kadanka et al. discussed above. In Particular, Mietus does not teach or suggest "a single component voltage pull-up device that is separate from said band-gap reference unit electronically coupled between said band-gap reference unit and said buffer circuit, wherein said single component voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference voltage and wherein said single component voltage pull-up device is implemented as a transistor" as is recited in the Claims 1, 7 and 16 (upon which Claims 6, 11, 15 and 23 depend respectively)

Applicant respectfully submits that nowhere in the Mietus reference is a single component voltage pull-up device that is separate from a band-gap reference unit that is electronically coupled between a band-gap reference unit and a buffer circuit, that acts to reduce a required supply voltage to maintain a band-gap reference voltage, and is implemented as a transistor as is set forth in Claims 1, 7 and 16 (upon which Claims 6, 11, 15 and 23 depend respectively) and disclosed in the Applicant's specification taught or suggested. Consequently, the embodiments of the claimed invention as are set forth in Claims 6, 11, 15 and 23 are neither anticipated nor rendered obvious by Kadanka et al. in view of Mietus.

Moreover, as it regards limitations recited in Claim 6, Applicant respectfully submits that nowhere in the Kadanka et al. and Mietus references is a method of responding to a request for a key of a first length that includes the above discussed limitation of Claim 1 and further includes the limitations "wherein said band gap reference voltage is provided by current through a transistor with a V_{BE} of less than 1.0 volts" as is recited in Claim 6 taught or suggested. Additionally, as it regards limitations recited in Claim 11, Applicant respectfully submits that nowhere in the Kadanka et al. and Mietus references is a method of responding to a request for a key of a first length that includes the above discussed limitation of Claim 1 and further includes

the limitations "wherein said transistor with a VBE of less than 1.0 volts is connected as an emitter follower" as is recited in Claim 11 taught or suggested.

Moreover, as it regards limitations recited in Claim 15, Applicant respectfully submits that nowhere in the Kadanka et al. and Mietus references is a method of responding to a request for a key of a first length that includes the above discussed limitation of Claim 1 and further includes the limitations "wherein said band gap reference voltage is provided by current through a transistor with a VBE of less than 1.0 volts" as is recited in Claim 15 (Claim 23 recites similar limitations) taught or suggested.

Because of the deficiencies of Kadanka et al. in view of Mietus discussed above, Applicant respectfully submits that Kadanka et al. in view of Mietus does not provide an adequate basis for rejection of Claims 1, 7 and 16 under 35 U.S.C. §103 and, as such, Claims 1, 7 and 16 are allowable. Accordingly, the Applicant respectfully submits that Claims 6, 11 and 15 and 23 dependent on Claims 1, 7 and 16 respectively, are likewise allowable as being dependent on allowable base claims.

CONCLUSION

In light of the foregoing amendments and remarks, Applicant respectfully submits that the remaining claims are in condition for allowance. Applicant respectfully requests allowance of the pending Claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

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Respectfully submitted,

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